WHAT IS CLAIMED IS:

1. A bootstrap diode emulator circuit for use with a half-bridge switching circuit, the switching circuit including low-side and high-side transistors connected to one another in a totem pole configuration at a load node, the low-side and high-side transistors having respective gate nodes; a driver circuit electrically coupled to the gate nodes of the low-side and high-side transistors, the driver circuit being controllable by at least one control input; a low-side voltage supply to produce a low-side voltage on a low-side supply node; and a bootstrap capacitor coupled between a high-side supply node and the load node, the bootstrap diode emulator circuit comprising:

an LDMOS transistor having a gate, a back-gate, a source and a drain, the drain of the LDMOS transistor being coupled to the high-side supply node, the source of the LDMOS transistor being coupled to the low-side supply node;

a gate control circuit electrically coupled to the gate of the LDMOS transistor, and

a dynamic back-gate biasing circuit electrically coupled to the back-gate of the LDMOS transistor;

wherein the gate control circuit is operable to turn on the LDMOS transistor in accordance with the at least one control input and the dynamic back-gate biasing circuit is operable to dynamically biases the back-gate of the LDMOS transistor when the LDMOS is turned on by applying a voltage to the back-gate of the LDMOS transistor that is close to but slightly lower than a voltage of the drain of the LDMOS transistor.

2. The bootstrap diode emulator circuit of claim 1, wherein the low-side and high-side transistors include one of FET devices and IGBT devices.

3. The bootstrap diode emulator circuit of claim 1, wherein the driver circuit includes low-side and high-side driver circuits respectively coupled to the gate nodes of the low-side and high-side transistors.

4. The bootstrap diode emulator circuit of claim 3, wherein the at least one control input includes a high-side control input and a low-side control input, the high-side driver being controllable by the high-side control input, the low-side driver being controllable by the low-side control input.

5. The bootstrap diode emulator circuit of claim 1, wherein the gate control circuit includes:

first and second transistors having respective source, drain, and gate nodes, the source of the first transistor being coupled to the drain of the second transistor at a first node, the drain of the first transistor being coupled to the gate of the LDMOS transistor, the source of the second transistor being coupled to the low-side return node;

a third transistor having source, drain, and gate nodes, the drain of the third transistor being coupled to the first node, the source of the second transistor being coupled to the low-side supply node;

a fourth transistor having source, drain, and gate nodes, the drain of the fourth transistor being coupled to the back-gate of the LDMOS transistor, the source of the fourth transistor being coupled to the low-side return node;

a first inverter having an input and an output, the input of the first inverter being coupled to the low-side control input, the output of the first inverter being coupled to the gates of the first, second, third, and fourth transistors;

a capacitor having first and second terminals, the first terminal of the capacitor being coupled to the gate of the LDMOS transistor;

a second inverter having an input and an output, the output of the second inverter being coupled to the second terminal of the capacitor;

a fifth transistor having source, drain, and gate nodes, the drain of the fifth transistor being coupled to the input of the second inverter, the source of the fifth transistor being coupled to the low-side supply node, the gate of the fifth transistor being coupled to the first node; and

a first current source having first and second terminals, the first terminal of the first current source being coupled to the input of the second inverter, the second terminal of the first current source being coupled to the low-side return node.

6. The bootstrap diode emulator circuit of claim 1, wherein the dynamic back-gate biasing circuit includes:

a first transistor having source, drain, and gate nodes, the gate node being coupled to the low-side control input via an inverter, the source of the first transistor being coupled to the low-side return node;

a second transistor having source, drain, gate, and back-gate nodes, the gate of the second transistor being coupled to the drain of the first transistor, the back-gate of the second transistor being coupled to the back-gate of the LDMOS transistor, the drain of the second transistor being coupled to the low-side supply node;

a first current source having first and second terminals, the first terminal of the first current source being coupled to the source of the second transistor, the second terminal of the first current source being coupled to the low-side return node;

a third transistor having source, drain, gate, and back-gate nodes, the source of the third transistor being coupled to the gate of the second transistor, the gate of the third transistor being coupled to the gate of the LDMOS transistor, the drain of the third transistor being coupled to the drain of the LDMOS transistor;

a second current source having first and second terminals, the first terminal of the second current source being coupled to the source of the third transistor, the second terminal of the second current source being coupled to the low-side return node; and

a PNP parasitic transistor having base, emitter, and collector nodes, the base of the parasitic transistor being coupled to the drain of the LDMOS transistor, the emitter of the parasitic transistor being coupled to the back-gate of the LDMOS transistor, the collector of the parasitic transistor being coupled to the low-side return node.

7. A half-bridge switching circuit to control low-side and high-side transistors electrically connected to one another at a load node in a totem pole configuration, the low-side and high-side transistors having respective gate nodes, a bootstrap capacitor being electrically coupled between a high-side supply node and the load node, the half-bridge switching circuit comprising:

a driver circuit electrically coupled to the gate nodes of the low-side and high-side transistors, the driver circuit being controllable by at least one control input;

a low-side voltage supply to produce a low-side voltage on a low-side supply node; and

a bootstrap diode emulator circuit coupled to the low-side supply node and including an LDMOS transistor having source, gate, drain, and back-gate nodes, the LDMOS transistor being controllable to supply the high-side supply node with a voltage approximately equal to the low-side voltage when the low-side driver is operated, the bootstrap diode emulator being operable to dynamically bias the back-gate node of the LDMOS transistor by applying a voltage to the back-gate of the LDMOS transistor that is close to but slightly lower than a voltage of the drain node of the LDMOS transistor.

8. The half-bridge switching circuit of claim 7, wherein the low-side and high-side transistors include one of FET devices and IGBT devices.

9. The half-bridge switching circuit of claim 7, wherein the driver circuit includes low-side and high-side driver circuits respectively coupled to the gate nodes of the low-side and high-side transistors.

10. The half-bridge switching circuit of claim 9, wherein the at least one control input includes a high-side control input and a low-side control input, the high-side driver being controllable by the high-side control input, the low-side driver being controllable by the low-side control input.

11. The half-bridge switching circuit of claim 7, wherein the bootstrap diode emulator further includes a gate control circuit operable to turn on the LDMOS transistor in accordance with the at least one control input, the gate control circuit including:

first and second transistors having respective source, drain, and gate nodes, the source of the first transistor being coupled to the drain of the second transistor at a first node, the drain of the first transistor being coupled to the gate of the LDMOS transistor, the source of the second transistor being coupled to the low-side return node;

a third transistor having source, drain, and gate nodes, the drain of the third transistor being coupled to the first node, the source of the second transistor being coupled to the low-side supply node;

a fourth transistor having source, drain, and gate nodes, the drain of the fourth transistor being coupled to the back-gate of the LDMOS transistor, the source of the fourth transistor being coupled to the low-side return node;

a first inverter having an input and an output, the input of the first inverter being coupled to the low-side control input, the output of the first inverter being coupled to the gates of the first, second, third, and fourth transistors;

a capacitor having first and second terminals, the first terminal of the capacitor being coupled to the gate of the LDMOS transistor;

a second inverter having an input and an output, the output of the second inverter being coupled to the second terminal of the capacitor;

a fifth transistor having source, drain, and gate nodes, the drain of the fifth transistor being coupled to the input of the second inverter, the source of the fifth transistor being coupled to the low-side supply node, the gate of the fifth transistor being coupled to the first node; and

a first current source having first and second terminals, the first terminal of the first current source being coupled to the input of the second inverter, the second terminal of the first current source being coupled to the low-side return node.

12. The half-bridge switching circuit of claim 7, wherein the boot strap diode emulator includes a dynamic back-gate biasing circuit operable to dynamically bias the back-gate of the LDMOS transistor when the LDMOS is turned on by applying the voltage to the back-gate of the LDMOS transistor that is close to but slightly lower than the voltage of the drain of the LDMOS transistor, the dynamic back-gate biasing circuit including:

a first transistor having source, drain, and gate nodes, the gate node being coupled to the low-side control input via an inverter, the source of the first transistor being coupled to the low-side return node;

a second transistor having source, drain, gate, and back-gate nodes, the gate of the second transistor being coupled to the drain of the first transistor, the back-gate of the second transistor being coupled to the back-gate of the LDMOS transistor, the drain of the second transistor being coupled to the low-side supply node;

a first current source having first and second terminals, the first terminal of the first current source being coupled to the source of the second transistor, the second terminal of the first current source being coupled to the low-side return node;

a third transistor having source, drain, gate, and back-gate nodes, the source of the third transistor being coupled to the gate of the second transistor, the gate of the third transistor being coupled to the gate of the LDMOS transistor, the drain of the third transistor being coupled to the drain of the LDMOS transistor;

a second current source having first and second terminals, the first terminal of the second current source being coupled to the source of the third transistor, the second terminal of the second current source being coupled to the low-side return node; and

a PNP parasitic transistor having base, emitter, and collector nodes, the base of the parasitic transistor being coupled to the drain of the LDMOS transistor, the emitter of the parasitic transistor being coupled to the back-gate of the LDMOS transistor, the collector of the parasitic transistor being coupled to the low-side return node.